ABSTRACT

In one embodiment, a central processing unit (CPU) includes multiple clock zones. Each clock zone includes at least one sensor that generates a signal indicative of a power supply voltage within the clock zone, a clock generator for providing a variable frequency clock to the clock zone, a first controller for controlling a frequency of operation of the clock generator in response to the at least one sensor, wherein the first controller further controls the frequency of operation in response to communication of frequency adjustments from first controllers in other clock zones within one cycle of latency, and a second controller that provides an overdrive signal, that is combined with adjustment signals from the first controller for the clock generator, in response to communication of frequency adjustments from other clock zones beyond one cycle of latency.